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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/464,297	12/15/1999	SHELDON ARONOWITZ	99-039	7342

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LSI LOGIC CORPORATION
1621 BARBER LANE
MS D-106, LEGAL DEPARTMENT
MILPITAS, CA 95035

EXAMINER
VINH, LAN

ART UNIT	PAPER NUMBER
1765	14

DATE MAILED: 06/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/464,297	ARONOWITZ ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4,7 and 9-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4,7 and 9-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 4, 7, 9-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al (US 6,284,149) in view of Kadomura (US 5,266,157)

Li discloses a plasma etching method to etch a silicon oxide layer 42 having a thickness formed on a semiconductor substrate in an etching chamber. This method comprises the steps of:

etching the oxide hard mask 42 of an integrated circuit formed on a semiconductor substrate using a plasma contains a substantial amount of nitrogen generated by a first RF power source 108, the power source is maintained at 1000 W (col 7, lines 34-36, col 10, lines 21-22, Table 1), which reads on exposing an oxide surface of an integrated circuit on a semiconductor substrate to a plasma consisting essentially of nitrogen generated by a first RF at a power level of from about 250-1000 W

applying an RF bias to the substrate holder from a second RF power source 84 maintained at a power level of 250 W during the step of etching the layer 42 using the nitrogen plasma (col 11, lines 15-27, Table 1)

Fig. 6 of Li shows a portion/a fixed thickness of the oxide layer 42 is removed during etching. Li also discloses that increasing the bias power also increase the etch rate (col

11, lines 3-5), which reads on the oxide thickness removed dependent upon the power level of the RF bias power.

Li differs from the instant claimed inventions as per claims 4, 11 by maintaining the RF bias power at a level of 250 W instead of a power level just below a level at which sputtering of the substrate material would commence on the semiconductor substrate/a power level ranging from above zero up to about 100 W as defined in page 3 of the specification.

However, Kadomura discloses a dry etching method comprise the step of etching a silicon oxide layer 3 using a nitrogen-containing plasma while maintaining the RF bias power at 100 W (col 4, lines 49-52, fig. 1B). Kadomura's teaching reads on maintaining the RF bias power at a power level just below a level at which sputtering of the substrate material would commence on the semiconductor substrate/a power level ranging from above zero up to about 100 W.

Since Li discloses that the bias power should be kept low (col 11, lines 3-4), one skilled in the art would have found it obvious to modify Li method by lowering Li's RF bias power level to a power level of about 100 W as per Kadomura because Kadomura teaches that with the RF bias power thus lowered, etching damages may also be lowered (col 5, lines 5-9)

Regarding claims 7, 14, Li discloses that the nitrogen plasma is generated by the first RF power source 108 located at a distance from the oxide surface 42 formed on semiconductor wafer/substrate 70 (fig. 8)

Regarding claim Li discloses maintaining the pressure in the etching chamber at 3-5 mT (table 1), which overlaps the claimed range of 1-1000 mT

Regarding claims 10, 16, 18, Li discloses forming oxide layer 42 covers the integrated circuit structure (fig. 5)

The limitation of claims 12, 14 have been discussed above.

Regarding claim 13, Li discloses using a RF source power of 250 W (Table 1)

Regarding claim 17, fig. 5 of Li shows an unmasked portion of layer 42/oxide layer is being etched by the nitrogen plasma.

3. Claims 19, 21- 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al (US 6,284,149) in view of Kadomura (US 5,266,157)

Li discloses a plasma etching method to etch a silicon oxide layer 42 having a thickness formed on a semiconductor substrate in an etching chamber. This method comprises the steps of:

placing the semiconductor wafer/substrate 70 on a substrate holder 72 in an etching chamber, the chamber maintained at a pressure of 3-5 mT (Fig. 8, Table 1) (3-5 mT overlaps the claimed range of 1-1000 mT)

etching the oxide hard mask 42 of an integrated circuit formed on a semiconductor substrate using a plasma contains a substantial amount of nitrogen generated by a first RF power source 108, the power source is maintained at 1000 W (col 7, lines 34-36, col 10, lines 21-22, Table 1), which reads on exposing an oxide surface of an integrated

circuit on a semiconductor substrate to a plasma consisting essentially of nitrogen generated by a first RF at a power level of from about 250-1000 W

applying an RF bias to the substrate holder from a second RF power source 84 maintained at a power level of 250 W during the step of etching the layer 42 using the nitrogen plasma (col 11, lines 15-27, Table 1)

Fig. 6 of Li shows a portion/a fixed thickness of the oxide layer 42 is removed during etching. Li also discloses that increasing the bias power also increase the etch rate (col 11, lines 3-5), which reads on the oxide thickness removed dependent upon the power level of the RF bias power.

Li differs from the instant claimed inventions as per claim 19 by maintaining the RF bias power at a level of 250 W instead of a power level ranging from above zero up to about 100 W.

However, Kadomura discloses a dry etching method comprise the step of etching a silicon oxide layer 3 using a nitrogen-containing plasma while maintaining the RF bias power at 100 W (col 4, lines 49-52, fig. 1B). Kadomura's teaching reads on maintaining the RF bias power at a power level just below a level at which sputtering of the substrate material would commence on the semiconductor substrate/a power level ranging from above zero up to about 100 W.

Since Li discloses that the bias power should be kept low (col 11, lines 3-4), one skilled in the art would have found it obvious to modify Li method by lowering Li's RF bias power level to a power level of about 100 W as per Kadomura because Kadomura

teaches that with the RF bias power thus lowered, etching damages may also be lowered (col 5, lines 5-9)

Regarding claim 21, Li discloses forming oxide layer 42 covers the integrated circuit structure (fig. 5)

The pressure of Li chamber of 3-5 mT, as shown in Table 1, overlaps the claimed pressure range of 1-200 mT

Regarding claim 23, Li discloses that the nitrogen plasma is generated by the first RF power source 108 located at a distance/remote located from the oxide surface 42 formed on semiconductor wafer/substrate 70 (fig. 8)

4. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al (US 6,284,149) in view of Kadomura (US 5,266,157) and further in view of Guinn et al (US 5,877,032)

Li as modified by Kadomura has been described above. Unlike the instant claimed invention as per claim 20, Li and Kadomura do not disclose the specific RF bias power level of above zero up to 50 W.

However, Guinn, in a method of dry etching, teaches that a process parameter such as bias power can be varied to change the etch rate (col 4, lines 4-6)

Hence, one skilled in the art would have found it obvious to modify Li and Kadomura by discovering the optimum value for the RF bias power level through routine experimentations because Guinn discloses that the bias power level is a result effective parameter/variable.

5. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al (US 6,284,149) in view of Guinn et al (US 5,877,032)

Li discloses a plasma etching method to etch a silicon oxide layer 42 having a thickness formed on a semiconductor substrate in an etching chamber. This method comprises the steps of:

etching the oxide hard mask 42 of an integrated circuit formed on a semiconductor substrate using a plasma contains a substantial amount of nitrogen generated by a first RF power source 108, the power source is maintained at 250 W (col 7, lines 34-36, col 10, lines 21-22, Table 1), which reads on exposing an oxide surface of an integrated circuit on a semiconductor substrate to a plasma consisting essentially of nitrogen generated by a first RF at a power level of from about 250-500 W

applying an RF bias to the substrate holder from a second RF power source 84 maintained at a power level of 250 W during the step of etching the layer 42 using the nitrogen plasma (col 11, lines 15-27, Table 1)

Fig. 6 of Li shows a portion/a fixed thickness of the oxide layer 42 is removed during etching. Li also discloses that increasing the bias power also increase the etch rate (col 11, lines 3-5), which reads on the oxide thickness removed dependent upon the power level of the RF bias power.

Li differs from the instant claimed inventions as per claim 24 by maintaining the RF bias power at a level of 250 W instead of a power level ranging from 10 to about 50 W.

However, Guinn, in a method of dry etching, teaches that a process parameter such as bias power can be varied to change the etch rate (col 4, lines 4-6)

Since Li discloses that the bias power should be kept low (col 11, lines 3-4), one skilled in the art would have one skilled in the art would have found it obvious to modify Li by discovering the optimum low value for the RF bias power level through routine experimentations because Guinn discloses that the bias power level is a result effective parameter/variable.

Response to Arguments

6. Applicant's arguments with respect to claims 4, 7, 9-24 have been considered but are moot in view of the new ground(s) of rejection.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 703 305-6302. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on 703 308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872-9310 for regular communications and 703 872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308-0661.

LV
May 29, 2003

BENJAMIN L. UTECH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700